AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1.-12 (cancelled).

13. (original): An integrated circuit package comprising:

a die pad having a first face and a second face opposite to said first face;

a plurality of leads each having a first face and a second face opposite to said first face, wherein

said plurality of leads is disposed substantially around at least a portion of said die pad, and

said first face of at least one of said plurality of leads has a recess formed therein, said recess having inner walls;

an integrated circuit chip having a first face and a second face opposite to said first face wherein said second face is coupled to said first face of said die pad;

a plurality of wires each linking said integrated circuit chip to one of said plurality of leads; and

an encapsulant enclosing said integrated circuit chip, said plurality of wires, said first face of said die pad, and a portion of said first face of each of said plurality of leads, wherein said encapsulant forms a plurality of side walls, and at least one of said side walls intersects said first face of said at least one of said plurality of leads between the inner walls of said recess formed therein.

14. (original): The integrated circuit package according to claim 13, wherein:

a majority of said plurality of leads has a recess formed therein, said recess having inner walls; and

said at least one of said plurality of side walls intersects said first face of said majority of said plurality of leads between the inner walls of said recess formed therein.

15. (original): The integrated circuit package according to claim 13, wherein said recess comprises a channel formed through said lead.

16. (original): The integrated circuit package according to claim 15, wherein said channel is formed from one side of the lead to the opposite side thereof.

17. (original): The leadframe according to claim 13, wherein said recess comprises a dimpleshaped impression.

18. (original): An integrated circuit package, comprising: a die pad;

a plurality of leads, each having a first face and a second face opposite to the first face, wherein at least on of said plurality of leads has a recess formed in said first face thereof, said recess having at least two inner walls;

an IC chip coupled to said die pad;

a plurality of wires connecting said integrated circuit chip to said plurality of leads; and

an encapsulant enclosing said integrated circuit chip, said plurality of wires, said dies pad, and a portion of at least one of said plurality of leads, wherein said encapsulant forms a plurality of side walls, at least one of which intersects said at least one lead between said inner walls of said recess formed therein, and wherein said encapsulant fills said recess.

19.-22. (cancelled).